**VLSI DSP 2017 Spring Homework Assignment #5**

Linear Regression module design

1. **Background**

Assume *X* is an independent variable and *Y* is a dependent variable, linear regression finds the linear relation between two variables by the following formula

 (1)

Given two data sequences  and , the two parameters of the linear regression, subject to the criterion of minimum mean square error, can be estimated as

 (2)

 (3)

The mean square error MSE can be calculated as

 (4)

1. **Design features**

Given two input data sequences  and , the linear regression module calculates the two parameters , and the MSE value. The hardware design should support the following features

* Capability of processing a continuous data flow, i.e., , and MSE should be computed on the fly along with the input data streams. At the end of the data streams, the computations should be completed as well ( a constant number of clock cycle delay, e.g. *m* clock cycles and *m* << *N*, is acceptable)
* The data sequence length *N* = 8 and the word length is 16 bits (MSB is the sign bit)
* Free of any line buffer or memory, just a few registers to hold the intermediate results are enough to complete the computations

1. **Design considerations**

To accomplish the aforementioned design features, several design issues must be resolved.

* The equations (2) ~ (4) should be reformulated so that they can be computed incrementally or on-the-fly with the advance of input data.
* For , this is easy as the accumulation (or the summation) can be performed incrementally
* For , although its value depends on the final outcome of , the two summation terms can still be computed incrementally. However, the completion of computation would be deferred until the availability of .
* After calculating  and , complete the MSE calculation.

1. **Hand in requirements**

The following items are required

* Circuit diagram of the derived design
* Verilog coding and verification results

1. **Due date**

* 2017/6/29 5PM